Vendor:ARM

Exam Code:EN0-001

Exam Name:ARM Accredited engineer

Version: Demo

QUESTION 1

Optimizing for space will:

A. Produce an image which is decompressed at run-time.

B. Cause the compiler to unroll loops where possible.

C. Result in more functions being inlined by the compiler.

D. Produce smaller code, even if this results in slower execution.

Correct Answer: D

QUESTION 2

Using a lower optimization level when compiling will:

A. Produce faster code.

B. Produce smaller code.

C. Produce non standard-compliant code.

D. Produce code that might be easier to debug.

Correct Answer: D

QUESTION 3

Which of the following ARM processors has the best energy efficiency (measured in mW/MHz)?

A. Cortex-M0+

B. Cortex-M4

C. Cortex-R4

D. Cortex-A15

Correct Answer: A

QUESTION 4

Within the ARMv7 architecture, which one of the following features is unique to the ARMv7-A profile?

A. Cache support

B. Privileged execution

C. The ARM instruction set

D. Virtual memory support

Correct Answer: D

QUESTION 5

Under which of the following circumstances is TLB maintenance always required?

A. If a TLB miss occurs

B. On every process switch

C. If the TLB reports a fault

D. When a page table entry is changed

Correct Answer: D

QUESTION 6

Which of the following functions can be performed by a spinlock?

A. Encrypting sensitive data on a network

B. Preventing interrupts from being received by a CPU

C. Preventing unauthorized access to an ARM powered device

D. Protecting a critical section or data structure from concurrent access

Correct Answer: D

QUESTION 7

Assume a little-endian system.

What is the value of R5 after the execution of the following piece of code?

```
LDR     R1, =0x100
LDR     R2, =0xAABBCCDD
STR     R2, [R1]
ADD     R1, R1, #0x2
LDRB    R5, [R1]
```

A. 0xBB

B. 0xAABBCC22

C. 0x102

D. 0xCC

Correct Answer: A

QUESTION 8

In which of these cases would code have better performance when compiled for Thumb state than when compiled for ARM state?

A. When the processor has no data cache

B. When the code involves many shifting operations

C. When the code has many conditionally executed instructions

D. When the processor can only fetch instructions 16-bits at a time

Correct Answer: D

QUESTION 9

In the Generic Interrupt Controller (GIC), when an interrupt is requested, but is not yet being handled, it is in which of the following states?

A. Inactive

B. Active

C. Pending

D. Edge-triggered

Correct Answer: C

QUESTION 10

Which of these items is typically shared between threads running in the same Operating System (OS) process?

A. Stack

B. Memory map

C. Register values

D. Program Counter

Correct Answer: B

QUESTION 11

Which one of the following statements is TRUE for software breakpoints?

A. Limited software breakpoints can be placed in code running from ROM

B. Each software breakpoint requires one watchpoint resource in the debug hardware

C. Each software breakpoint requires one breakpoint resource in the debug hardware

D. The number of available software breakpoints is not limited by the debug hardware

Correct Answer: D

QUESTION 12

In a loop termination test, how might a programmer indicate to the compiler that the loop iteration count limit is divisible by four?

A. AND the count limit with -0x3

B. Add 4 to the count limit

C. Subtract 4 from the count limit

D. Shift the count limit left two bit positions

Correct Answer: A